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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,686	03/08/2004	David E. Freker	42P19260	2635

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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 08/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,686	FREKER ET AL.	
	Examiner	Art Unit	
	Hau H. Nguyen	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) *1-10 and 18-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-17 and 30-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The response filed on June 23, 2006 has been fully considered in preparing for this Office Action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 11-17, and 30-33, 37-39, 41-42, 45-47 are rejected under 35 U.S.C. 102(b) as being anticipated by Aleksic et al. (U.S. Patent No. 6,469,703).

Referring to claims 11 and 30, as shown in Figs. 1 and 7, Aleksic et al. teach a computer system comprising a graphics controller 640, a dual channel memory 140 (Figs. 1 and 4), a central processing unit 110, a memory controller 630 coupled to the CPU via data router 620, to the dual channel memory 140, and to the graphics controller 640. As shown in Fig. 5, Aleksic et al. teach the memory locations of channels CH0 and CH1 partitioned into blocks, which are logically addressed by channels CH0 and CH1. In the embodiment shown, the blocks are accessed by CH0 and CH1 in an alternating manner. For example, block 0 (first sequence of pairs of consecutive data blocks), as illustrated in table 5 of FIG. 5, is accessed by channel CH0; block 1, which is horizontally adjacent to block 0, is accessed by channel CH1; the next horizontally adjacent block, block 2, is accessed by channel CH0. In this alternating manner, different data channels access horizontally adjacent data blocks associated with the first row of

memory (row 0). In the specific embodiment of FIG. 4, the horizontally adjacent channels have adjacent physical addresses, in that the last memory location of block 0 is immediately adjacent to the first memory location of block 1 (col. 6, lines 1-16).

In regard to claims 12 and 13, because each block of data shown in Fig. 5, (block 0, 1,...) can be interpreted as pairs of consecutive data block, the first sequence of pairs consists of odd pairs, and the second sequence consists of even pairs. If the pairs of blocks are number sequentially, the first memory channel stores a pair of blocks 0, 1 and a pair of blocks 4, 5, and the second memory channel stores a pair of blocks 2 and 3, and a pair of blocks 6 and 7.

In regard to claims 14-15, 31-32, with reference again to Fig. 5, after block 4, or block 9, or block E, the first memory channel CH0 and the second memory channel CH1 reverses the order (see also col. 6, lines 17-36). Since the first sequence and second sequence reverse their order after a transition interval, the first sequence consists of even pairs, and the second sequence consists of odd pairs.

As for claims 16 and 17, Aleksic et al. also teach the memory mapping is assigned by the graphics controller (col. 8, lines 60-63).

As per claim 33, Aleksic et al. teach mapping the first through six pairs of data alternatively in the first and second memory channels in sequential and reverse orders as cited above.

As per claims 37 and 38, Aleksic et al. teach the memory controller 630 detects devise coupled to the memory controller (such as CPU or graphics engine 640, Fig. 7), selects a primary device from among the detected devices for memory access (such as CPU), and selects a system

memory memory map to optimize system memory operation with the selected device (col. 7, line 64 to col. 8, line 7, col. 8, lines 25-30, and col. 9, lines 17-32).

As per claim 39, as shown in Fig. 8, Aleksic et al. further teach selecting a primary device (clients 0-n), and determining a memory configuration for the graphics controller (e.g. via channel 0 or channel 1, col. 9, lines 39-50).

As per claim 41, Aleksic et al. teach selecting a system memory map to optimize graphics memory access if the graphics controller is selected (col. 5, lines 55-67).

As per claim 42, as cited above, Aleksic et al. teach the adjacent data blocks of the first pair have adjacent address values.

As per claims 45 and 46, Aleksic et al. also teach the data blocks are accessible to a graphics controller and data can be written into the memory from the graphics controller 640 (Fig. 7, and col. 7, lines 43-63).

As per claim 47, Aleksic et al. teach the first and second sequence of pairs are simultaneously accessible (col. 10, lines 6-10).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 34-36, 40, 43, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aleksic et al. (U.S. Patent No. 6,469,703).

In regard to claims 34-36, although Aleksic et al. fail to explicitly teach the data block is a quadword, it would have been obvious to one skilled in the art to utilize the method of mapping data block as taught by Aleksic et al., such that each data block is a quadword because by doing so, data access and retrieval can be faster in one memory access cycle, and thus, optimizing overall performance.

In regard to claim 40, as cited above, Aleksic et al. teach selecting either the CPU or the graphics controller to access the memory device (as illustrated in Fig. 7), wherein the CPU has the priority to access the memory (col. 9, lines 17-33), and the graphics controller can access system memory as cited above. Although Aleksic et al. fail to explicitly teach the graphics controller having internal memory, it would have been obvious to one skilled in the art to include a local memory in the graphics controller in order to temporarily store data being processed without accessing system memory during the CPU access.

As per claim 43, with reference to Fig. 5, although Aleksic et al. do not explicitly teach the size of each block, it would have been obvious to one skilled in the art to modify the data block as taught by Aleksic et al. such that the size of each block is 8 bytes by 8 bytes, which is a typical graphics data block. Thus, by the configuration as shown in Fig. 5, if the first data block (of block 0) consists of 8 bytes (a fixed number of bytes) and is accessed by the first channel 0, and if the first data block (of block 5) consists of 8 bytes and is accessed by the second channel 1, then the two data block are spaced apart by eight times the fixed number of bytes.

As per claim 44, although Aleksic et al. do not explicitly teach the interleaved memory is double data rate memory device, it would have been obvious to one skilled in the art to use one,

because double data rate memory device is well known in the art, and is used to provide faster data transfer.

Response to Arguments

Applicant's arguments filed 06/23/2006 have been fully considered but they are not persuasive. In response to Applicant's argument that the cited reference Aleksic et al. (U.S. Patent No. 6,469,703) (hereinafter, Aleksic) does not teach "pairs of consecutive data blocks," the examiner disagrees. In fact, as an example shown in Fig. 5, Aleksic teaches alternating storing a first sequence of pairs of consecutive data blocks (first byte of block 0) in the first channel (channel 0), and storing a second sequence of pairs of consecutive data blocks (first byte of block 5) in the second channel (channel 1) in sequential order (col. 6, lines 50-65). Thus, one "byte" as taught by Aleksic can be interpreted as "a sequence of pairs of consecutive (4-bit) data blocks."

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-2 17-9197 (toll-free).

H. Nguyen

08/24/2006

KEE M. TUNG
SUPERVISORY PATENT EXAMINER